REMARKS / ARGUMENTS

This application contains Claims 1-15. Claims 1-7 and 10 were rejected; claims 8, 9, 11-15 were objected to, the latter claims being allowable if placed in proper form.

Claims 1 and 3-7 were provisionally rejected under judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1-3, 5-6 and 13 of co-pending Application No. 10/052,620. The Examiner takes the position that such conflicting claims are not patentably distinct from each other because the claims of the instant application are broader than those of 10/052,620 and, therefore, that the claims of this application are envisioned by 10/052,620.

Claims 1-7 were also provisionally rejected for the same reason above on obviousness-type double patenting as being unpatentable over Claims 1-8 of co-pending Application No. 10/052,619. In this case the Examiner states that "the microdendritic pad array of Claim 1 reads on a device chip."

The above noted rejections are made with respect to co-pending Application Nos. 10/052,620 and 10/052,619. These applications describe chip carriers and microjoint structures that are somewhat related. However, the claimed structures of the several applications are not identical and, in fact, they are patentably distinct because they define differently the carrier and microjoint structures of the co-pending applications. In particular, the "microdendritic pad array" is solely a feature of the 10/052,619 application. See Figure 4, layer 28.

There are, of course, similar receptacles on the carriers, but the present application teaches the use of distinct raised stud structures which enables easy assembly between the carrier and device array via those receptacles in the carrier and device array. The stud and cooperating pad scheme of the application constitutes a unique structure, different from the solder balls used in connection with the chip devices found in the 10/052,620 application. Each stud comprises "a non-fusible post" made of a material, such as copper, with a coating of a fusible material or alloy – like solder – at its end. This quoted language has been added to Claims 1 and 10 herein.

It will be appreciated that the total scheme, as now clearly defined, for example, in Claim 1, uniquely allows easy placement of the chip devices on the carrier and allows for small

variations in the planarity of the carrier, such that a reliable bond between the studs and the receptacles can be achieved over the entire chip and circuit assembly.

Accordingly, with the amendment of Claims 1 and 2 there can be no question that there is no basis for rejection of Claims 1 and 3-8 for double patenting in the light of Application 10/052,620; nor for the rejection of Claims 1-7 for double patenting because of 10/052,619.

Certain claims are also rejected on the prior art, specifically Claims 1-2 and 10 are rejected under 35 U.S.C.102(b) as being anticipated by Jackson et al (3,942,245). The Examiner commented specifically with regard to elements similar to applicant's construction, but the Jackson patent instead of studs simply has a pair of solder balls 19 on the device 20 at each connection location.

In order to make abundantly clear that applicant's construction and concept is totally distinct, Claim 1 has been thoroughly amended to include the specific recital of the nature of the studs in sub-paragraph 2:

> including conductive studs extending outwardly above the surface of said pads, the studs being individual non-fusible posts formed to match in spatial location with each of the respective receptacles on said chip carrier.

It is important to point out that the term "microjoint" used in reference to applicant's construction is defined as a structure which permits a very high density of so-called interconnections; for example, well below 10μm pitch down to the very small 10-micron pitch and involving even feasible down to 2.5 micron pitch if required. See particularly page 2, line 3 to page 3, line 2 of applicant's specification. Also, page 7, lines 1-2.

With respect to the rejection on the Brown patent, the distinction between that reference and applicant's construction is likewise now manifest, there being absolutely no set of microjoint pads including studs as now precisely defined; nor is there anything comparable to the matched spatial relationship of the studs with respective receptacles.

It is to be noted that the cited patents deal with chip attachment to flexible lead frames or flexible membranes and are typically used at pad sizes and wiring feature sizes that are at least 50 to 100 times coarser than the ones envisioned in this application. Moreover, the structures

described in these patents are used to alleviate mechanical strains due to assembly and thermal processing, resulting from the mounting of silicon chips on circuit boards or other polymeric substrates. In contra-distinction thereto, the structure taught in the present application is targeted for use at ground rules typical in semi-conductor fabrication, and involves joining the device chips onto a chip carrier with such fine features extending up to the top surface. Hence, we denote the chip carrier distinctly as a microjoint carrier (microjoint having been defined previously).

The Examiner refers to the cavities or recessed regions described in the prior art patents as equivalent to the receptacles taught in this application. These features in the prior art patents are generated by mechanically bending the lead frame to form a crank area or by cutting out large sections of the substrates such as the circuit board. The receptacles disclose herein are regions photo-lithographically produced on the microjoint chip carrier to have small sizes and are matched in scale to the fine-sized raised studs on the device chips.

Accordingly, since it will now be apparent that all the claims of this application unequivocally define applicant's invention over the art of record and are clearly and patentably distinct over the claims of the related applications, this application is in condition to be passed to issue.

Respectfully submitted,

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